High speed ADC: one that no one had ever told you

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The performance of a band HF receiver, direct RF samples are decided by two or three maker ADC high speed, in the world.
But only Linear Technology produces ADC with bits effective bits, ENOB, of constant value versus frequency. It is what allows for the same values of MDS (at equal bandwith) from 1.8 to 30 MHz or 50 MHz) with ideal local oscillator**.**

The best design is the one that has the smallest possible **Delta**.
Where Delta is = SNR real receiver - SNR ADC (without pre-amplifier in front ADC)

Absolute limits of NF and Clip level of the best ADC for Receiver Full DSP with max frequency.
Under these conditions:
a) Oscillator Phase noise = infinite dBc and white noise from 100 -200 kHz (corner frequency) to 120 MHz= -174 dBm/Hz (NF =0 dB). In this conditions rms Jitter = 0 fS
b) Delta = 0 dB

	LTC 2208 14BIT	LTC 2208- 16 BIT
Sample's frequency	120 MHz	120 MHz
Nyquist's frequency	60 MHz	60 MHz
Noise Power in Nyquist band.	-77. 8 dBm	- 77. 8 dBm
Minimun SINAD (S+D)/N @ 30 MHz	75.1 dB-	75.9 dB-
Effective Number of Bits, ENOB	12. 1	12. 3
Sensitivity and Bit loss ADC	11. 4 dB 1.9 bit	22.2 dB 3.7 bit
Clip Level = Max input signal power with driver Gain = 0 dB. 50 ohm sbil Input out 800 ohm bil.	10. 4dBm	10.4 dBm
Noise Figure, NF	31. 5 dB	30.7 dB
MDS@500 Hz CW	-115.5 dBm	-116. 1 dBm
MDS@2400Hz SSB	-110.7 dBm	-111. 3 dBm
Acquisition delay time jitter	70 fS	70 fS
Price from >100 pieces	77. 65 $	91. 65 $

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You can view that a move from 14-bit to 16-bit phisically the gain is **only 0.8 dB with an ideal OL and an ideal project.**

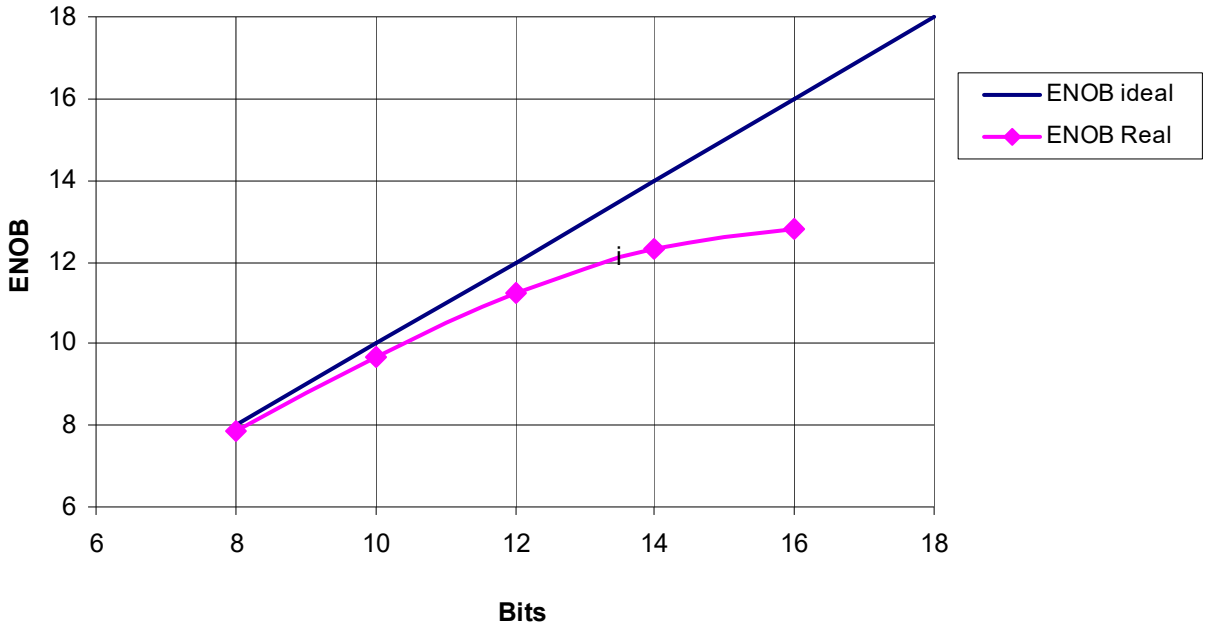
Into practice with real oscillator and Delta designer a receiver with 14 bit ADC can be better than an RX with 16-bit ADC.

Today we reached 12.8 EN0B. Acquisition time delay Jitter = 45 fS
with $ 180 (100+pz): LTC2107

I calculated the SNR real of ADC the best in the word with the following data:
1) Acquisition time delay Jitter = 45 fS
2) Average differential nonlinearity, DNL = + - 0.5 bits
3) Effective input noise generated by the ADC 1.9
Input frequency = 30 MHz.
N: Number bit phisically

By setting 1) = 0 , 2)= 0 and 3) = 0 you get the SNR ideal
From SNR ideal and SNR real it obtained the EN0B real and ideal
and they were represented in the graph

This is the comparison of ENOB ideal with EN0B real.
You will understand why there are no ADC to 18 bits High speed.
The case is a small capacitor into block: Sample& Hold



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COMPARISON **ONLY NF AND CLIP LEVEL** OF RX OF PERSEUS (MEASURED BY I2VGO-2008) AND IC7300(MEUSURED BY NC0B. 4/10/ 2016 EMAIL TO I2VGO)		
Specification	**Perseus LTC 2206 14 bit**	**IC 7300 -LTC 2208 14 bit**-
Sample's frequency	80 MHz	120 MHz
Nyquist's frequency	40 MHz	60 MHz
Noise Power in bandwith Nyquist	-77.8dBm	-76 dBm
Minimum SIND (S+D)/N	75.7 dB- at 15 MHz	75.1 dB-at 30 MHz
Effective Number of Bits, EBNO	12.3	12.2
Acquisition delay time jitter	80 fS	70 fS
Pre off with bench filter preselector		
Noise Figure BDR @10kHz	20 dB. 117 dB,	25 dB 101 dB
Clip level	-3.5 dBm	-9 dBm
Pre 1 On		
Noise Figure BDR @10kHz	19 dB ?	6dB ?
Clip Level	-7 dBm	-22 dBm
- Pre 2 On		
Noise Figure BDR @10kHz	----------	5 dB ?
Clip Level		-26 dB
Pre off and IP+Off		
Noise Figure BDR @10kHz	------	12 dB 81 dB
Clip Level		-9 dBm
year supply	September 2007	April 2016

Reference
Analog-Digital Conversion, Walt Kester; Analog Devices Inc ISBN 0-916550-27-3 (2004)

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Cause error of the value " Acquisition delay time jitter" of ADC KT 2208- 14 deleted my previous document dated: 4/14/2016.